AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Original) A method of compensating for accumulated data-dependent post-manufacture shift in a characteristic of one or more of a pair of matched devices within an integrated circuit, said shift giving rise to a mismatch in the characteristic between the pair of matched devices, the method comprising:

preconditioning the matched devices to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected magnitude of any further lifetime shift in the characteristic of either matched device.

2. (Original) The method, as recited in claim 1, wherein the respective initial shift in each of the matched devices is substantially equal.

3. (Original) The method, as recited in claim 1, wherein the respective initial shift in the characteristic in each of the matched devices is greater than the an expected magnitude of any remaining lifetime shift in the characteristic of either matched device.

4. (Original) The method, as recited in claim 1, wherein the preconditioning step comprises subjecting each of the matched pair of devices to substantially equal time durations of a predetermined bias condition known to promote the shift in the characteristic.

5. (Original) The method, as recited in claim 1, wherein the preconditioning step is carried out at an elevated temperature to promote the shift in the characteristic.

6. (Original) The method, as recited in claim 4, wherein:
the matched devices comprise field effect transistors; and
the predetermined bias condition includes a negative gate-to-source voltage.

7. (Original) The method, as recited in claim 4, wherein the preconditioning step comprises subjecting the matched pair of devices to substantially equal time durations of a first

bias condition corresponding to one data state as a second bias condition corresponding to another data state opposite the one data state.

8. (Original) The method, as recited in claim 4, wherein the preconditioning step comprises subjecting both matched devices simultaneously to the predetermined bias condition.

9. (Original) The method, as recited in claim 5, wherein the preconditioning step is performed during a burn-in operation.

10. (Original) The method, as recited in claim 1, wherein the preconditioning step is carried out at an elevated temperature and for a period of time sufficient to cause a respective initial shift in each of the matched devices which are substantially equal in magnitude and greater than the an expected magnitude of any remaining lifetime shift in the characteristic of either matched device.

11. (Currently Amended) The method, as recited in claim 10, wherein:

the matched devices form a portion of a sensing circuit of a semiconductor memory; and

the preconditioning step comprises subjecting the matched pair of devices to substantially equal time durations of a first bias condition corresponding to one data state as a second bias condition corresponding to another data state opposite the one data state.

12. (Original) The method, as recited in claim 11, wherein said one data state and said another data state are conveyed serially on a test data bus.

13. (Original) The method, as recited in claim 1, wherein:

the matched devices form a portion of a sensing circuit of a semiconductor memory; and

the at least one characteristic susceptible to an accumulated data-dependent mismatch results, at least in part, from an effect that disparately affects one of the pair of matched devices as compared with the other, the disparate effect based on a skew in a history of values read out from associated memory elements.

14. (Original) The method as recited in claim 13 wherein the disparate effect is associated with negative bias temperature instability.

15. (Original) The method as recited in claim 13 wherein the disparate effect involves a monotonic change in the characteristic based on disparate voltage bias histories of the matched devices.

16. (Original) The method as recited in claim 15 wherein the characteristic is mobility.

17. (Original) The method as recited in claim 15 wherein the characteristic is threshold voltage (V_t).

18. (Original) The method as recited in claim 13 wherein:
the pair of matched devices comprises PMOS transistors;
the characteristic is threshold voltage (V_t); and
the disparate effect is associated with negative bias temperature instability and results in a monotonic increase in V_t based on disparate voltage bias histories of the PMOS transistor devices.

19. (Original) The method as recited in claim 18 wherein the pair of matched devices comprises cross-coupled PMOS load devices.

20. (Original) The method, as recited in claim 19, wherein the preconditioning step comprises subjecting each of the cross-coupled PMOS load devices to substantially equal time durations of a negative gate-to-source voltage.

21. (Original) The method, as recited in claim 20, wherein the preconditioning step comprises individually subjecting each of the cross-coupled PMOS load devices to substantially equal time durations of the negative gate-to-source voltage.

22. (Original) The method, as recited in claim 20, wherein the preconditioning step comprises subjecting both cross-coupled PMOS load devices simultaneously to the negative gate-to-source voltage.

23. (Original) The method as recited in claim 18 wherein the preconditioning step is performed during a burn-in operation.

24. (Original) A circuit comprising:

first and second matched devices which are susceptible to an accumulated data-dependent post-manufacture shift in a characteristic of one or more of the matched devices, said shift giving rise to a mismatch in the characteristic between the matched devices; and

a preconditioning circuit for subjecting the matched devices to a particular condition for a length of time sufficient to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected magnitude of any further lifetime shift in the characteristic of either matched device.

25. (Original) The circuit, as recited in claim 24, wherein:

the first and second matched devices together comprise a cross-coupled pair of transistors within a sensing circuit of a semiconductor memory.

26. (Original) The circuit, as recited in claim 25, wherein:

the cross-coupled pair of transistors comprise PMOS transistors.

27. (Original) The circuit, as recited in claim 24, wherein the preconditioning circuit comprises means for applying a substantially uniform bias history across both first and second matched devices.

28. (Original) The circuit, as recited in claim 24, wherein the preconditioning circuit comprises means for subjecting each of the matched devices to substantially equal time durations of a predetermined bias condition known to promote the shift in the characteristic.

29. (Original) The circuit, as recited in claim 28, wherein:
the matched devices comprise field effect transistors; and
the predetermined bias condition includes a negative gate-to-source voltage.

30. (Original) The circuit, as recited in claim 28, wherein the preconditioning circuit is arranged to subject the matched devices to substantially equal time durations of a first bias condition corresponding to one data state as a second bias condition corresponding to another data state opposite the one data state.

31. (Original) The circuit, as recited in claim 30, wherein said one data state and said another data state are conveyed serially on a test data bus.

32. (Currently amended) The circuit, as recited in claim 28, wherein ~~wherein~~ the preconditioning circuit is arranged to subject both matched devices simultaneously to the predetermined bias condition.

33. (Original) The circuit, as recited in claim 28, wherein the preconditioning circuit is configured to be enabled during a burn-in operation.

34. (Original) The circuit, as recited in claim 24, wherein the at least one characteristic susceptible to an accumulated data-dependent mismatch results, at least in part, from an effect that disparately affects one of the pair of matched devices as compared with the other, the disparate effect based on a skew in a history of values read out from associated memory elements.

35. (Original) The circuit, as recited in claim 34, wherein the disparate effect is associated with negative bias temperature instability.

36. (Original) The circuit, as recited in claim 34, wherein the disparate effect involves a monotonic change in the characteristic based on disparate voltage bias histories of the matched devices.

37. (Original) The circuit, as recited in claim 36, wherein the characteristic is mobility.

38. (Original) The circuit, as recited in claim 36, wherein the characteristic is threshold voltage (V_t).

39. (Original) The circuit, as recited in claim 34, wherein:

the matched devices comprise PMOS transistors;

the characteristic is threshold voltage (V_t); and

the disparate effect is associated with negative bias temperature instability and results in a monotonic increase in V_t based on disparate voltage bias histories of the PMOS transistor devices.

40. (Original) The circuit, as recited in claim 39, wherein the pair of matched devices comprises cross-coupled PMOS load devices within a sensing circuit of a semiconductor memory.

41. (Original) The circuit, as recited in claim 40, wherein the preconditioning circuit is configured to subject each of the cross-coupled PMOS load devices to substantially equal time durations of a negative gate-to-source voltage.

42. (Original) The circuit, as recited in claim 41, wherein the preconditioning circuit is configured to individually subject each of the cross-coupled PMOS load devices to substantially equal time durations of the negative gate-to-source voltage.

43. (Original) The circuit, as recited in claim 41, wherein the preconditioning circuit is configured to subject both cross-coupled PMOS load devices simultaneously to the negative gate-to-source voltage.

44. (Original) The sensing circuit, as recited in claim 39, wherein the preconditioning circuit is configured to be enabled during a burn-in operation.

45. (Original) The circuit of claim 24 embodied within a sensing circuit of a memory integrated circuit.

46. (Original) The circuit of claim 24 embodied within a sensing circuit of a processor integrated circuit including memory or cache.

47. (Original) The circuit, as recited in claim 24, embodied as a sensing circuit in computer readable descriptive form suitable for use in design, test, or fabrication of an integrated circuit.

48. (Original) An integrated circuit comprising:

memory elements;

a sense amplifier circuit for sensing data stored in associated memory elements, said sense amplifier including first and second matched devices which are susceptible to an accumulated data-dependent post-manufacture shift in a characteristic of one or more of the matched devices, said shift giving rise to a mismatch in the characteristic between the matched devices; and

a preconditioning circuit for subjecting the matched devices to a particular condition for a length of time sufficient to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected magnitude of any further lifetime shift in the characteristic of either matched device.

49. (Original) The integrated circuit, as recited in claim 48, wherein:

the first and second matched devices together comprise a cross-coupled pair of transistors within a sensing circuit of a semiconductor memory.

50. (Original) The integrated circuit, as recited in claim 49, wherein:

the cross-coupled pair of transistors comprise PMOS transistors.

51. (Original) The integrated circuit as recited in claim 48 wherein the at least one characteristic susceptible to an accumulated data-dependent mismatch results, at least in part, from an effect that disparately affects one of the first load devices as compared with the other,

the disparate effect based on a skew in a history of values read out from associated memory elements.

52. (Original) The integrated circuit as recited in claim 51 wherein the disparate effect is associated with negative bias temperature instability.

53. (Original) The integrated circuit as recited in claim 51 wherein

the matched devices are PMOS devices;

the characteristic is threshold voltage (V_t); and

the disparate effect involves a monotonic increase in V_t based of disparate voltage bias histories of the PMOS devices.

54. (Original) The integrated circuit of claim 48 embodied as a semiconductor memory.

55. (Original) The integrated circuit of claim 48 embodied as a processor integrated circuit including memory or cache.

56. (Original) A computer readable encoding of a semiconductor integrated circuit design, the computer readable encoding comprising:

one or more media encoding a representation of a memory circuit that includes plural pairs of bit lines, memory cells coupled to respective ones of the bit line pairs;

the one or more media further encoding a representation of a sense amplifier circuit coupled to one or more respective ones of the bit line pairs for sensing data stored in associated memory elements, said sense amplifier circuit including first and second matched devices which are susceptible to an accumulated data-dependent post-manufacture shift in a characteristic of one or more of the matched devices, said shift giving rise to a mismatch in the characteristic between the matched devices; and

the one or more media further encoding a representation of a preconditioning circuit for subjecting the matched devices to a particular condition for a length of time sufficient to cause an initial shift in the characteristic in each of the matched

devices and to thereby reduce an expected magnitude of any further lifetime shift in the characteristic of either matched device.

57. (Original) The computer readable encoding of claim 56 wherein each of the one or more media are selected from the set of a disk, tape or other magnetic, optical, semiconductor or electronic storage medium and a network, wireline, wireless or other communications medium.

58. (Original) The computer readable encoding of claim 56, in combination with one or more respective media readers therefor, wherein the one or more media and respective media readers, when combined, are exercisable to supply an information stream suitable to at least partially define one or more process steps for fabrication of semiconductor integrated circuits in accordance with the encoded design.